Response under 37 C.F.R. 1.116
Applicant: Jose L. Cervantes
Serial No.: 10/025,165
Filed: December 19, 2001
Docket No.: 10002896-1
Title: PORTABLE COMPUTER HAVING DUAL CLOCK MODE

REMARKS

The following Remarks are made in response to the Final Office Action mailed October 26, 2005, in which claims 1-24 and 28-31 were rejected. Claims 1-24 and 28-31 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 103

Claims 1-24 and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui, U.S. Patent No. 6,763,478 ("Bui") in view of Kelly, U.S. Patent No. 6,336,166 ("Kelly).

Applicant submits that it would not be obvious to one skilled in the art to combine the teachings of Bui either alone or in view of the secondary reference Kelly and arrive at the present invention of claims 1-24 and 28-31.

Bui discloses a computer system that includes a high performance clock frequency and a low performance clock frequency depending on whether battery or AC power is used. (See Bui, Abstract). When operating in low performance mode, FSB 105 bus frequency and memory bus 95 frequency will be set to 66 MHz. In high performance mode the two buses will operate at 100 MHz. (See Bui, column 5, lines 10-13.) The North Bridge ASIC 30 relays the clock frequency signal, either 66 MHz or 100 MHz, as a clock frequency signal represented by memory clock signal 75. The memory clock signal 75 is sent to the memory clock buffer 80, and the clock frequency is passed on as a memory clock signal 85 to SDRAM memory 90. (See Bui, column 5, lines 37-42).

Kelly discloses a computer memory access and control system, which includes a cache line buffer for ROM and an independent ROM bus. (See Kelly, column 1, lines 57-59). The computer memory access and control system also employs a ROM bus 205 that is separate and independent of the random access memory (RAM) buses, for example, RAM buses 210 and 215. (See Kelly, Figure 2, column 3, lines 22-30). With a separate ROM data path, that includes a full cache line buffer, memory access operations are more efficiently conducted because a RAM access (i.e., a read or write operation) and a ROM access (i.e., a read operation) can be executed concurrently (See Kelly, Abstract).

Applicant submits that Bui, either alone or in view of Kelly, fails to disclose, teach or suggest the invention of independent claim 1. Bui fails to disclose **a second memory bus.** See Examiner's Remarks Office Action, page 3. Further, Bui fails to disclose **a control**

system coupled to the first memory bus and the second memory bus, wherein the control system is configured to operate the first memory bus and the second memory bus at a first speed in the first power mode and a second speed different than the first speed in the second power mode.

Kelly also fails to disclose **a control system coupled to the first memory bus and the second memory bus, wherein the control system is configured to operate the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different than the first speed in the second power mode.** Kelly merely shows a ROM bus that is separate from the random access memory (RAM) bus. Accordingly, one could not combine the teachings of Bui either alone or in combination with the teachings of Kelly and arrive at the present invention of independent claim 1.

Further, neither Bui nor Kelly, teach or suggest **a control system configured to operate the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different than the first speed in the second power mode.** Again, Bui discloses ASIC 30 coupled to SDRAM memory 90 via memory bus 95. Kelly merely discloses a ROM bus 205 separate from RAM buses 210 and 215 to allow concurrent memory access. Kelly also fails to suggest operating **the first memory bus and the second memory bus at a first speed in the first power mode, and a second speed different from the first speed in the second power mode.** As such, it also would not be obvious to one skilled in the art to apply the teachings of Bui, in view of Kelly and arrive at the invention of independent claim 1. Similar limitations are included in independent claims 11, 17, 21, and 28. Accordingly, Applicant requests that the above rejection of independent claims 1, 11, 17, 21, and 28 under 35 U.S.C. § 103 be withdrawn.

Dependent claims 2-10, 12-16, 18-20, 22-24, and 29-31 further define patentably distinct claim 1, 11, 17, 21, or 28. Accordingly, Applicant believes these dependent claims are also allowable. Allowance of claims 1-24 and 28-31 is respectfully requested.

In addition, claims 5 and 13 recite **wherein the second bus speed is double the first bus speed.** The Examiner cites Bui at column 5, lines 3-13 as teaching this limitation. (Office Action, page 6). Bui, however, discloses that when operating in low performance mode, FSB 105 bus frequency and memory bus 95 frequency will be set to 66 MHz. In high performance mode the two busses will operate at 100 MHz. (Column 5, lines 10-13). The

100 MHz speed is clearly not double the 66 MHz speed. Therefore, Bui and Kelly, either alone, or in combination, fail to teach or suggest the limitations of claims 5 and 13.

Further, claim 30 recites **wherein the performance level input is configured to allow a user to select a user defined memory bus speed for the first clock speed and the second clock speed.** The Examiner cites Bui at column 2, lines 4-11 as teaching this limitation. (Office Action, page 9). Bui, however, discloses that if the user wants increased performance, although the system is running on battery and low performance mode, the user can go to high performance mode by initiating the applet and forcing the CPU to go to high performance mode. (Column 2, lines 7-11). Bui clearly teaches only two bus speeds, one for the low performance mode and one for the high performance mode. Neither of these bus speeds can be defined by the user. The bus speeds are set to 66 MHz and 100 MHz. (See Bui, column 5, lines 3-13). Bui fails to teach **a user defined memory bus speed.** Therefore, Bui and Kelly, either alone, or in combination, fail to teach or suggest the limitations of claim 30.

In addition, it appears the Examiner has failed to address claim 31. Claim 31 recites **wherein the performance level input is configured to include a power mode over-ride setting for the first battery power mode and the second power mode, including allowing a user to select between a slow memory bus speed, a fast memory bus speed, or a user-defined memory bus speed.** For the same reasons as discussed above with reference to claim 30, Bui fails to teach these claim limitations. While Bui allows a user to select between a low performance mode and a high performance mode, Bui does not allow a user to select a user-defined memory bus speed. Therefore, Bui and Kelly, either alone, or in combination, fail to teach or suggest the limitations of claim 31.

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CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-24 and 28-31 are all in a condition for allowance and requests reconsideration of the application and allowance of all pending claims.

Any inquiry regarding this Amendment and Response should be directed to either Gregg W. Wisdom at Telephone No. (360) 212-8052, Facsimile No. (360) 212-3060 or Steven E. Dicke at Telephone No. (612) 573-2002, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this paper or papers, as described herein, are being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (571) 273-8300 on this 21 day of November, 2005.

By Steven E. Dicke
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